

SBND will have more than 11 thousand channels all being digitized at a rate of 2 MHz with a 12-bit resolution. At 270 Gbps, this presents a tall order for both data transfer and storage, and it precludes full-reconstruction-based readout decisions. One way to select interesting events is to incorporate a system that issues signals based on logical combinations of detector signals (i.e. a hardware trigger) that represent particular event types. Hardware triggers are both fast and can be made reasonably complex via the use of Field-Programmable Gate Arrays (FPGAs).

The Penn Trigger Board (PTB) is a printed circuit board, designed at Penn, to fan in various signals from the detector subsystems and translate them to a common logic flavor that an FPGA can understand. The PTB serves as a carrier to a Microzed which is a commercial board that hosts a System on a Chip (SoC) with an embedded FPGA. The SoC soft core is capable of running a Linux distribution that in SBND, will allow for remote access to configuration files and trigger definitions and will be able to transfer data directly to the Data Acquisition (DAQ) system.

The end goal of this project is to integrate the PTB into the DAQ chain, allowing SBND to make trigger-based readout decisions utilizing the status of its detector subsystems. Specifically, this project will involve commissioning the trigger hardware, developing fpga code that meets trigger requirements, and writing software that relays the trigger information to the DAQ.